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A NOVEL STRATEGY FOR MULTILEVEL CASCADED INVERTERS (MLCI) UNDER UNBALANCED DC SOURCES

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Abstract: **This paper introduces a pulse width-modulation strategy to achieve balanced line-to-line output voltages and to maximize modulation index over the range of linear modulation where the output voltage can be linearly adjusted in the multilevel cascaded inverter (MLCI) functioning under unbalanced dc-link conditions. In these conditions, the linear modulation range is lowered, and a considerable output voltage imbalance may occur as voltage references increase. In order to study these effects, the voltage vector space for MLCI is examined in detail. From this analysis, the theory behind the output voltage imbalance is analyzed, and the maximum linear modulation range obtainable taking into consideration an unbalanced dc-link condition is evaluated. Thereafter, a strategy based on neutral voltage modulation is introduced to obtain the output voltage balance and as to extend the linear modulation range up to the maximum point in theory. In this method, very large dc-link imbalance distorts the balancing of the output voltages. This limitation is also discussed. The simulation for a seven-level phase-shifted modulated MLCI for electric vehicle traction drive illustrate that the proposed method proves to be efficient in balancing the line-to-line output voltages and also in maximizing the range of linear modulation involving the unbalanced dclink conditions.**
Keywords: Linear **Modulation Range, MLCI, PWM.**

I.INTRODUCTION

Multilevel inverters enable the synthesis of a sinusoidal output voltage from several steps of voltages. Owing to this factor, the multilevel inverters have low *dv/dt* ratings and usually have low harmonics in the output voltage and current. Also, the switching of very high voltages is made possible by stacking of multilevel inverter modules. Due to these advantages, multilevel inverters have been applied in various application fields. Among various multilevel inverters schematics, the multilevel cascaded inverter (MLCI) topology is one of the prominent topologies due to its simple design for modularization and tolerance to faults. The modulation strategy in MLCI applications, to generate gate signals is very crucial to achieve high-performance control.

In most cases, PWM strategy based on carrier or SVPWM is suited for applications such as motor drives, where dynamic properties are very important, while SHEPWM strategy is suitable for some high-power static power conversion applications. To reduce the common-mode voltage, a multilevel SVPWM has been proposed. The series SVPWM method has been reported to easily implement SVPWM for the MLCI. Normally, SVPWM is implemented for hybrid inverters consisting of neutral point clamp and Hbridge inverters in order to improve output voltage efficiency and quality. As with two-level inverters, it is also possible to operate carrier-based SVPWMs which are proportional to traditional SVPWMs by injecting a common offset voltage to the three-phase references MLCIs require distinct dc links. Hence, if there are one or more faults present in the dc links in respective phase or in cases asymmetry is observed in the voltage magnitudes of the dc links, the output voltage of the MLCI can be unbalanced without proper compensation. In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to mitigate the imbalance in magnitude of output voltage and an offset voltage to extend the linear modulation range, can be calculated. In the present method, very large dc-link imbalance precludes the

output voltages from being balanced. Therefore, if this scheme is applied to applications such as EV traction systems, the dynamic characteristics can be greatly improved.

II.SYSTEM DESCRIPTION

The MLCI- based inverter for EV Traction Drive is shown in fig 1 below.

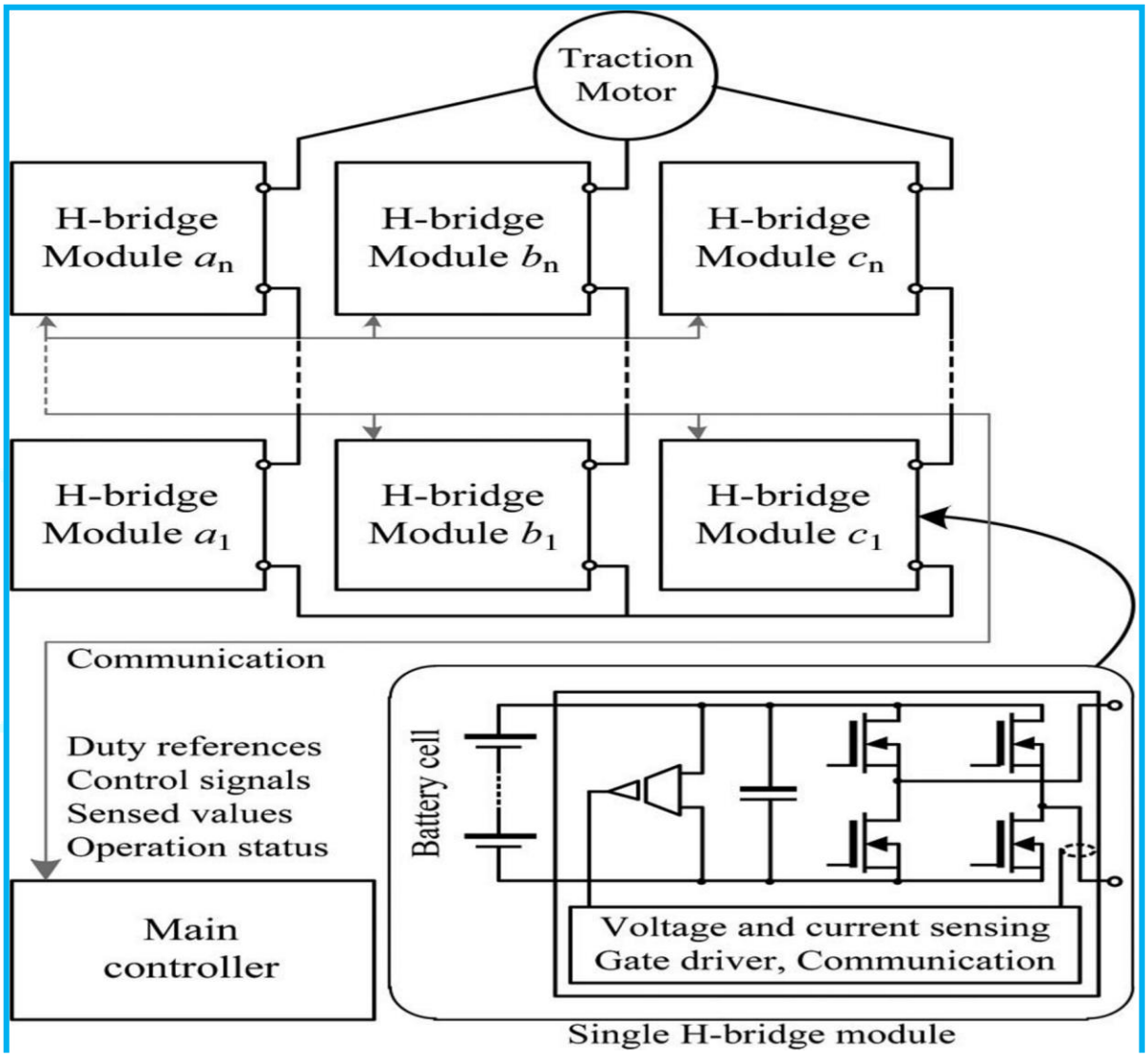

Fig. 1. MLCI-based inverter for EV traction drive.

In this configuration, various power ratings can be easily implemented by configuring the number of the single H-bridge modules according to a required specification such as an EV traction drive, sedan, and so on. Here, each H-bridge module has voltage and current sensors, gate drives, and communication interfaces between the module itself and the main controller. It also consists of battery cells. The unipolar modulation technique is applied in the H-bridge module between two switching legs. As a result of this, the effective switching frequency in each H-bridge module is two times that of the carrier frequency. In addition to this, the well-known PS modulation technique is used to implement multilevel operation.

Therefore, the effective switching frequency *f*sw in a phase is

$$Fsw = 2N \times fc \quad (1)$$

Where *N* and *fc* represent the number of the H-bridge modules in each phase and the carrier frequency of PWM, respectively. Fig. 2 below illustrates the carriers for each module, the duty cycles in unipolar modulation, and the output voltage when *N* = 2.

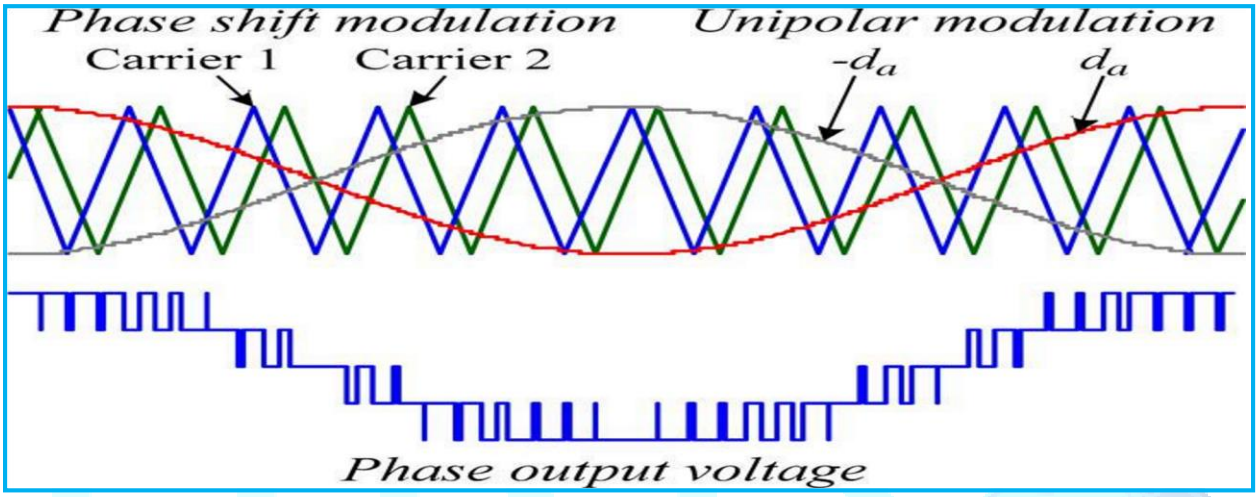

Fig. 2. Unipolar and phase shift modulation for single H-bridge module.

III.PROPOSED NOVEL STRATEGY FOR MLCI CASCADED INVERTERS UNDER UNBALANCED DC SOURCES

A novel strategy is proposed to realize the maximum value of modulation index in the range of linear modulation under the unbalanced conditions. The offset voltage injection scheme is a famous technique in three-phase half-bridge inverter applications. The principle behind this is that an offset voltage is incorporated with phase voltage references to implement various PWM schemes in carrier-based PWM by making use of the fact that line-to-line voltages are applied to a three-phase load [1], [2]. Consider, the offset voltage *v* sn* is used to the phase voltage references *v*as*, *v*bs*, and *v*cs* to implement carrierbased SVPWM as in

$$v_{sn}^{*} = \frac{v_{\max}^{*} + v_{\min}^{*}}{2} \qquad v_{\max}^{*} = \max\left(v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\right) \quad (2)$$

$$v_{\min}^{*} = \min\left(v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\right).$$

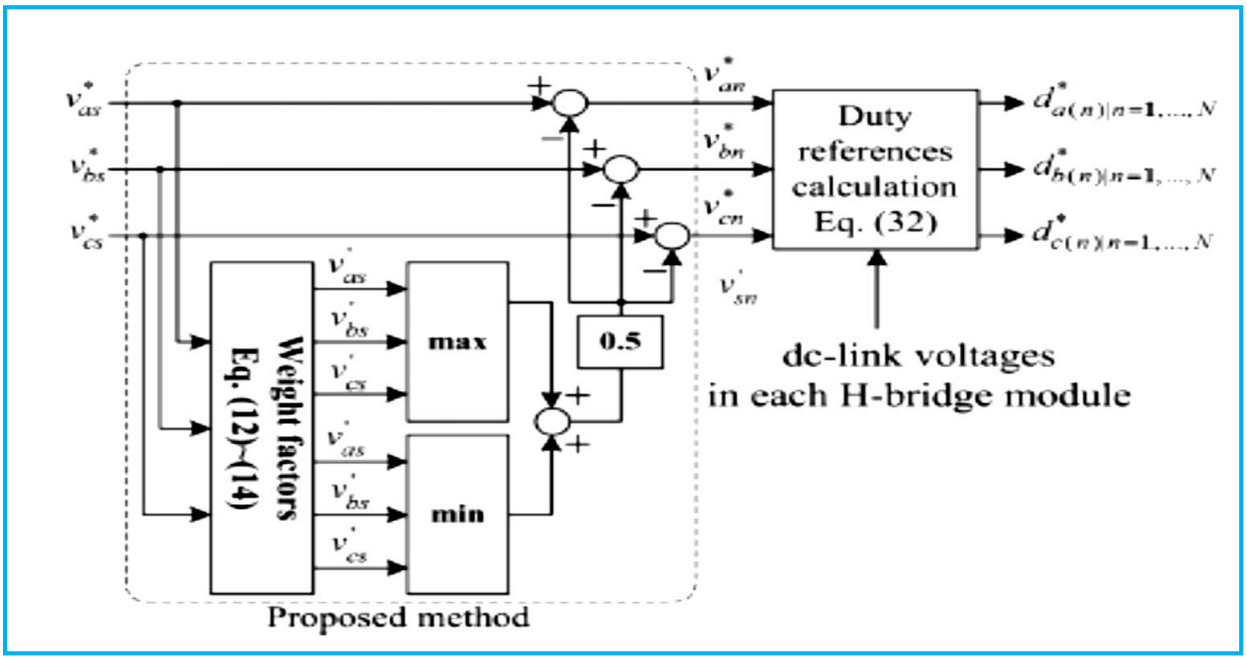

Fig. 3. Implementation of the NVM Method.

Now, the voltage references at pole i.e.*v* an*, *v*bn*, and *v*cn*, which will be converted to PWM duty references, are

$$v_{an}^{*}=v_{as}^{*}-v_{sn}^{*} \quad v_{bn}^{*}=v_{bs}^{*}-v_{sn}^{*} \quad v_{cn}^{*}=v_{cs}^{*}-v_{sn}^{*}. \tag{3}$$

In case the unbalanced dc links in an MLCI and the conventional offset voltage injection methods are utilized, the three-phase output voltages would be distorted due to the factor that the phase voltage reference approaches *V*ph_max. This is because the traditional methods do not take into account dc-link conditions when unbalanced. Therefore, even if a phase can synthesize the reference voltage at output in the range of linear modulation, the remaining phases can besaturated or go into the over modulation region. In this condition, a neutral voltage can be developed by the saturated or overmodulated phase. In order to resolve this issue and to synthesize the output voltage to *V*ph_max in the range of linear modulation, the NVM technique is proposed in this paper. Fig. 3 shows the concept of the proposed NVM technique.

The neutral voltage between the two neutral points *n* and *s* is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. Making use of this fact, the proposed method lowers the portion of the phase whose dc-link voltage is lower than the others and maximizes the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, *v'sn* does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one obtained from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. Also, if all the voltages of dc-link are well balanced so that *V*dc_*a*, *V*dc_*b*, and *V*dc_*c* are equal to *V*dc.

IV.SIMULATED PERFORMANCE

A simple one-by-three configuration MLCI model is built in Matlab Simulink. The three-phase *RL* load with R = 0.1Ωand L = 1mH is employed. The dc-link voltages for each phase are Vdc_a = 0.5 × 30 V, Vdc_b = 0.75 × 30 V,and Vdc_c = 30 V. The maximum synthesizable phase voltage in linear is

$$V_{\mathrm{ph\_max}} = \frac{0.75 \times 30 + 0.5 \times 30}{\sqrt{3}} = 21.65 \text{ V}. \tag{4}$$

The voltage references are given by

$$\begin{aligned} v_{as}^{*} &= V_{\mathrm{ph\_max}} \sin(100\pi t) \\ v_{bs}^{*} &= V_{\mathrm{ph\_max}} \sin(100\pi t - 2\pi/3) \\ v_{cs}^{*} &= V_{\mathrm{ph\_max}} \sin(100\pi t + 2\pi/3). \end{aligned} \tag{5}$$

The conventional SVPWM gives more area than SPWM.However, the voltage distortion is unavoidable. This method shows no distortion in the output voltage and maximizes the voltage vector space compared to other methods.The time-domain simulation results are illustrated below.The time range from$t$ = 0.0 secs to$t$ = 0.05 secs, the conventional SPWM is used. The time range from t = 0.05 secs to$t$ = 0.1 secs, conventional SVPWM is used. After the time t = 0.1 secs, the proposed method is applied. With conventional SVPWM, the voltage *v*sn* is not zero anymore, and the peak value of the pole voltage references is reduced compared to SPWM. But in both cases, the duty reference of phase *a*, where the dclink voltage is least among the three phases, is saturated. Whileusing the proposed method however, the duty references are not saturated because the fundamental frequency component of the neutral voltage is included in *v*sn*.

The benefit of the proposed method can be analyzed from the peak value of the phase current in the final part of the figure. Under conventional methods, the phase currents are unbalanced. But,with the proposed method the phase currents are well balanced. From the simulation outputs, it is clear that the proposed method can obtain the maximum obtainable phase voltage in the linear modulation range under unbalanced dc link.

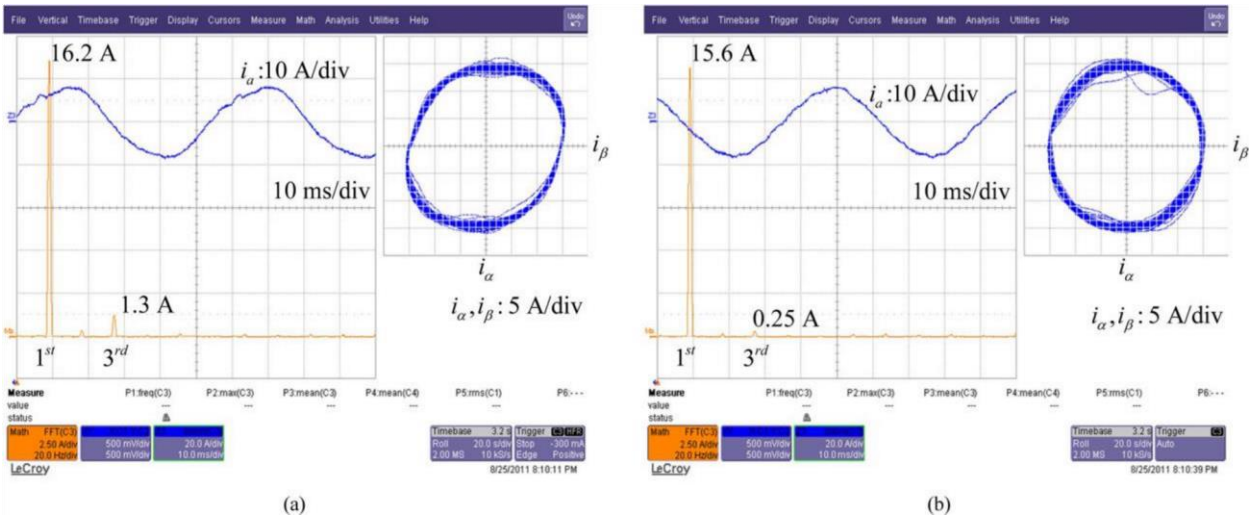

Fig. 4. Comparison of the FFT results and the current trajectories in the *α−β* plane. (a) Traditional carrierbased SVPWM. (b) Proposed NVM.

V.CONCLUSION

The NVM technique under unbalanced dc-link conditions for MLCIs has been proposed in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the analysis of voltage vector space is done using the switching function. This proves that the maximum linear modulation range was derived. The proposed NVM technique is used to obtain the maximum modulation index in the linear modulation range under an unbalanced dc-link condition and also to balance the output phase voltages. Compared to the previous methods, the proposed technique is easy to implement and the output voltage quality profile under unbalanced dc-link conditions is improved. Both simulations and experimental results conducted on the IPM motor drive application verify the effectiveness of the proposed method.

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